

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)	
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Ming-Ren Lin et al.)	Group Art Unit: Unassigned
)	
Divisional Application of)	Examiner: Unassigned
Application Serial No.: 10/405,343)	
)	
Filed: April 16, 2004)	
)	
Title: METHOD FOR FORMING)	
STRUCTURES IN FINFET DEVICES)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicant(s) bring to the attention of the Examiner the documents listed on the attached PTO 1449. This Information Disclosure Statement (IDS) is being filed before the mailing date of a first Office Action in the above-referenced application. As such, no certification or fee is required. Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not attached, because such documents were either cited by the Examiner or properly submitted in an IDS in the parent application, Application No. 10/405,343, filed April 3, 2003.

Applicant(s) respectfully request(s) that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

If any copending application(s) is/are cited on the attached PTO 1449, the Examiner's attention is directed to the foregoing application(s) in compliance with § 2001.06(b) of the Manual of Patent Examining Procedure. By identifying the copending application(s), the assignee and/or applicant of the application(s) do not waive confidentiality of the application(s). Accordingly, the U.S. Patent and Trademark Office is requested to maintain the confidentiality of the copending application(s) under 35 U.S.C. § 122.

This submission does not represent that a search has been made and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and Applicant(s) determine(s) that the cited document(s) do not constitute "prior art" under United States law, Applicant(s) reserve(s) the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

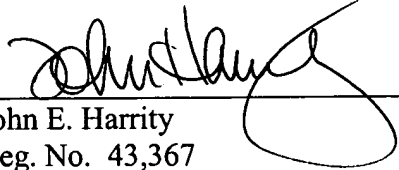
Applicant(s) further reserve(s) the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 50-1070.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: _____


John E. Harrity
Reg. No. 43,367

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800
Customer Number: 26615

Date: April 16, 2004

INFORMATION DISCLOSURE CITATION PTO-1449		Customer Number 26615	ATTORNEY'S DKT No. H1417D		DIVISIONAL APPLICATION OF APPLICATION SERIAL No. 10/405,343	
			APPLICANT(S) Ming-Ren Lin et al.			
			FILING DATE APRIL 16, 2004		GROUP Unassigned	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,645,797 B1	11-11-03	Buynoski et al.	438	157	12-06-02
	6,583,469 B1	06-24-03	Fried et al.	257	329	01-28-02
	6,562,665 B1	05-13-03	Yu	438	149	10-16-00
	6,537,880 B1	03-25-03	Tseng	438	260	09-13-01
	6,514,819 B1	02-04-03	Choi	438	253	02-26-99
	6,492,212 B1	12-10-02	leong et al.	438	157	10-05-01
	6,413,802 B1	07-02-02	Hu et al.	438	151	10-23-00
	6,358,827 B1	03-19-02	Chen et al.	438	585	01-19-01
	6,232,622 B1	05-15-01	Hamada	257	67	09-28-99
	6,180,441 B1	01-30-01	Yue et al.	438	197	05-10-99
	5,932,911	08-03-99	Yue et al.	257	330	12-13-96
	5,705,414	01-06-98	Lustig	437	41	12-23-96

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424.
	Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886.
	Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
	Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
	Co-pending U.S. Patent Application Serial No. 10/726,569, filed December 4, 2003, titled "SYSTEMS AND METHODS FOR FORMING MULTIPLE FIN STRUCTURES USING METAL-INDUCED-CRYSTALLIZATION," 23 pages.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

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			APPLICANT(S) Ming-Ren Lin et al.		
			FILING DATE APRIL 16, 2004	GROUP Unassigned	

U.S. PATENT DOCUMENTS						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,338,959	08-16-94	Kim et al.	257	331	03-30-93
	4,996,574	02-26-91	Shirasaki	357	23.7	06-30-89

FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Co-pending U.S. Application Serial No. 10/754,515 and Preliminary Amendment, filed January 12, 2004 titled "FinFET Device With Multiple Fin Structures."
	Co-pending U.S. Application Serial No. 10/755,344 and Preliminary Amendment, filed January 13, 2004 titled "FinFET Device With Multiple Channels."
	U.S. Patent Application Publication No. US 2003-0178677 A1, September 25, 2003, Clark et al.

EXAMINER	DATE CONSIDERED
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